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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,276	01/14/2002	Goro Nakatani	040894-5755	4701
9629	7590	06/23/2010	[REDACTED]	EXAMINER
MORGAN LEWIS & BOCKIUS LLP			[REDACTED]	IM, JUNGHWA M
1111 PENNSYLVANIA AVENUE NW			[REDACTED]	ART UNIT
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/043,276	NAKATANI ET AL.
<b>Examiner</b>	<b>Art Unit</b>	
JUNGHWA M. IM	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 11 March 2010.
- 2a) This action is **FINAL**.      2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1,3 and 8-15 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1,3 and 8-15 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 14 January 2002 is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____ .	6) <input type="checkbox"/> Other: _____ .

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 3 and 8-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 6410414) in view of Braeckelmann et al. (US 6218302), hereinafter Braeckelmann and Ting et al. (US 5169680), hereinafter Ting.

Regarding claims 1, Fig. 6 of Lee shows semiconductor device comprising:  
a first interconnect layer (102) arranged above a substrate (100) on which a functional semiconductor device is formed (100; active region; col.3, lines 5-10);  
an inter layer dielectric (104) directly covering a portion of top surface and the side surfaces of the first interconnect layer;  
a silicon nitride film (106; col.3, line 28) formed so as to cover entirely a top surface of said interlayer dielectric,  
a metal interconnect layer (110) covering over said silicon nitride film; and  
a planarized polyimide (116; col. 5, lines 47-52) which is formed directly on a Surface of the silicon nitride film and directly surrounding the metal interconnect layer including a side wall thereof,

wherein a portion of the planarized polyimide is removed at a part of a region of the metal interconnect layer and an interconnection (114) is connected to the region of the metal interconnect layer.

Fig. 6 of Lee shows substantially the entire claimed structure except the metal interconnect layer (the uppermost metal layer) made of gold serving as a bonding pad and a polyimide layer covering a surface and a side wall of the gold layer. Fig. 11 of Braeckelmann shows the uppermost metal layer (83) made of gold serving as a bonding pad and a polyimide layer (1001, 1002) covering a surface and a side wall of the gold layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Braeckelmann into the device of Lee in order to have the top metal interconnect layer consisting of gold to increase the conductivity, and to have a bond wire connected to the exposed region of the metal interconnect layer to accommodate the connection of the functional semiconductor device with wires. Note that Fig. 11 of Braeckelmann shows a portion of the polyimide passivation layer is removed to expose the portion of the gold layer.

The combination of Lee/Braeckelmann shows most aspects of the instant invention except “wherein the inter layer dielectric includes a first inter layer dielectric formed on the first interconnect layer and a second inter layer dielectric formed on a periphery of the first interconnect layer, and the first inter layer dielectric is thinner than the second inter layer dielectric, and wherein a sum of a thickness of the first interconnect layer and a thickness of the first inter layer dielectric is substantially same as a thickness of the second inter layer dielectric.” Fig. 5 of Ting shows the inter layer

dielectric (27) includes a first inter layer dielectric formed on the first interconnect layer (21) and a second inter layer dielectric formed on a periphery of the first interconnect layer, and the first inter layer dielectric is thinner than the second inter layer dielectric, and wherein a sum of a thickness of the first interconnect laver and a thickness of the first inter layer dielectric is substantially same as a thickness of the second inter layer dielectric. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Ting into the device of LeeBraeckelmann in order to have the inter laver dielectric including a first inter layer dielectric formed on the first interconnect layer and a second inter layer dielectric formed on a periphery of the first interconnect layer, and the first inter layer dielectric being thinner than the second inter layer dielectric, and wherein a sum of a thickness of the first interconnect laver and a thickness of the first inter layer dielectric is substantially same as a thickness of the second inter layer dielectric to reduce the device size.

Regarding claim 3, “high-density plasma CVD” is a process designation, and would thus not carry patentable weight in this claim drawn to a product. *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 8, Fig. 6 of Lee shows semiconductor device comprising:  
a first interconnect layer (102) arranged above a substrate (100) on which a functional semiconductor region is formed (100);  
an inter layer dielectric (104) directly covering a portion of top surface and the side surfaces of the first interconnect layer;

a silicon nitride film (106; col.3, line 28) formed so as to cover entirely a top surface of said interlayer dielectric,

a metal interconnect layer (110) covering over said silicon nitride film; and a planarized polyimide (116; col. 5, lines 47-52) which is formed directly on a surface of the silicon nitride film and directly surrounding the metal interconnect layer including a side wall thereof,

wherein a portion of the planarized polyimide is removed at a part of a region of the metal interconnect layer and an interconnection (114) is connected to the region of the metal interconnect layer.

Fig. 6 of Lee shows substantially the entire claimed structure except the metal interconnect layer (the uppermost metal layer) made of gold, a barrier layer covering the contacting hole and a portion of a surface of the silicon nitride film around the contacting hole, thereby forming a barrier layer region and a projection area of the metal interconnect layer connected with a bonding wire is overlapped with said functional semiconductor device. Fig. 11 of Braeckelmann shows said metal interconnect layer (83) being consist of gold material, a barrier layer (81) covering the contacting hole and a portion of a surface of the interlayer insulating film (73) around the contacting hole, thereby forming a barrier layer region, and a projected area of the metal interconnect layer connected to a bond wire (104) is overlapped with the functional semiconductor device. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Braeckelmann into the device of Lee in order to have the top metal interconnect layer consisting of gold to increases the conductivity

and to have a barrier layer region for improved conductivity, and further to have a bond wire connected to the region of the metal interconnect layer to accommodate the connection of the functional semiconductor device with wires.

Note that Fig. 11 of Braeckelmann shows a portion of the polyimide passivation layer is removed to expose the portion of the gold layer.

The combination of Lee/Braeckelmann shows most aspects of the instant invention except “wherein the inter laver dielectric includes a first inter layer dielectric formed on the first interconnect layer and a second inter layer dielectric formed on a periphery of the first interconnect layer, and the first inter layer dielectric is thinner than the second inter layer dielectric, and wherein a sum of a thickness of the first interconnect laver and a thickness of the first inter layer dielectric is substantially same as a thickness of the second inter layer dielectric.” Fig. 5 of Ting shows the inter laver dielectric (27) includes a first inter layer dielectric formed on the first interconnect layer (21) and a second inter layer dielectric formed on a periphery of the first interconnect layer, and the first inter layer dielectric is thinner than the second inter layer dielectric, and wherein a sum of a thickness of the first interconnect laver and a thickness of the first inter layer dielectric is substantially same as a thickness of the second inter layer dielectric. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Ting into the device of LeeBraeckelmann in order to have the inter laver dielectric including a first inter layer dielectric formed on the first interconnect layer and a second inter layer dielectric formed on a periphery of the first interconnect layer, and the first inter layer dielectric being thinner than the

second inter layer dielectric, and wherein a sum of a thickness of the first interconnect layer and a thickness of the first inter layer dielectric is substantially same as a thickness of the second inter layer dielectric to reduce the device size.

Regarding claim 9, Braeckelmann discloses that the barrier layer consists of titanium (col. 3, lines 8-11).

Regarding claims 10 and 11, Braeckelmann discloses the first interconnect layer (124) consists of aluminum (col. 3, lines 20-30).

Regarding claim 12, Braeckelmann discloses the inter layer dielectric consists of USG film (col. 3, lines 47-54).

Regarding claim 13, Fig. 11 of Braeckelmann shows the functional semiconductor region further comprises a polysilicon gate (108) isolated from the first interconnect layer by a second dielectric layer (110), wherein the first interconnect layer is connected to the polysilicon gate through a contacting area disposed within the second dielectric layer.

Regarding claims 14 and 15, Fig. 11 of Braeckelmann shows the planarized polyimide is removed only at the part of the region of the surface of the metal interconnect layer, thereby the metal interconnect layer includes a part of the surface exposed from the planarized polyimide and a part of the surface coated with the planarized polyimide.

***Response to Arguments***

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JUNGHWA M. IM whose telephone number is (571)272-1655. The examiner can normally be reached on MON.-FRI. 7:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/  
Supervisory Patent Examiner, Art  
Unit 2811

/J. M. I./  
Examiner, Art Unit 2811

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